Notice of Allowability	Application No.	Applicant(s)	
	10/092,129	ERNST ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed on 02/02/2005*.

2. ☒ The allowed claim(s) is/are *1-10*.

3. ☒ The drawings filed on *06 March 2002* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

RD

DETAILED ACTION

1. Claims 1-10 are pending in this application and have been examined. Claim 1 has been amended.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Attorney Richard E. Jenkins on May 5, 2005.

Please amend the application as follows:

As per the Specification:

Page 1, line 11, change "US 6 031 692" to "US 6 038 692".

As per the Abstract on page 18:

Please delete the phrase at lines 3 and 4 of the Abstract.

Please replace the paragraph at line 6 of the Abstract with the following amended paragraph:

- - ~~Address~~ An address generator is provided for generating addresses for testing an addressable circuit. The address generator can include a base address register for buffer-storing a base address. The base address register can be assigned an

associated offset register group having a plurality of offset registers for buffer-storing relative address values. Further, the address generator can include a first multiplexer circuit which is dependent on a base register selection control signal, switches through an address buffer-stored in the base address register to a first input of an addition circuit and to an address bus, which is connected to the circuit to be tested. A second multiplexer circuit can be dependent on the base register selection control signal, through-connects the offset register group associated with the through-connected base address register to a third multiplexer circuit, which is dependent on an offset register selection control signal. ~~(2), having: at least one base address register (12) for buffer-storing a base address, the base address register (12) in each case being assigned an associated offset register group (13) having a plurality of offset registers for buffer-storing relative address values; a first multiplexer circuit (38), which, in a manner dependent on a base register selection control signal, switches through an address buffer-stored in the base address register (12) to a first input (59) of an addition circuit (60) and to an address bus (3), which is connected to the circuit (2) to be tested; a second multiplexer circuit (17), which, in a manner dependent on the base register selection control signal, through-connects the offset register group (13) associated with the through-connected base address register (12) to a third multiplexer circuit (25), which, in a manner dependent on an offset register selection control signal, through-connects an offset register of the through-connected offset register group (13) to a second input (61) of the addition circuit (60); the addition circuit (60) adding the address~~

~~present at the first input to the relative address value present at the second input (61) to form an address which is buffer-stored in the base address register (12).~~ - -

Please delete the phrase "Figure 4" at line 33 of the Abstract.

Response to Arguments

3. Applicant's arguments, see Applicant Remarks, filed February 2, 2005, with respect to claims 1-10 have been fully considered and are persuasive. The Examiner has withdrawn the rejection of claims 1-10 as a result of Applicant's amendment of February 2, 2005.

Allowable Subject Matter

4. Claims 1-10 are allowed.

The following is an Examiner's Statement of Reason for Allowance.

The present invention pertains generally to an address generator for generating addresses for testing an addressable circuit, and in particular for testing an addressable memory module.

The claimed invention as set forth in claim 1 recites features such as: An address generator for generating addresses to test an addressable circuit. The address generator can have at least one base address register (such as one of a plurality of base address registers 12a, 12b, etc. shown in Figure 4) for buffer-storing a base address. The base address register in each case can be assigned an associated offset register group (such as offset register group 13a and 13b shown in Figure 4) having a

plurality of offset registers (for example, offset register group 13a has offset registers 13a-1, 13a-2, etc. shown in Figure 4) for buffer-storing relative address values. The address generator also has a first multiplexer circuit, which, in a manner is dependent on a base register selection control signal, switches through an address buffer-stored in the base address register to a first input of an addition circuit and to an address bus, which is connected to the circuit to be tested. In addition, the address generator can include a second multiplexer circuit, which, in a manner is dependent on the base register selection control signal, through-connects the offset register group associated with the through-connected base address register to a third multiplexer circuit. The third multiplexer circuit is dependent on an offset register selection control signal, through-connects an offset register of the through-connected offset register group to a second input of the addition circuit. Further, the addition circuit adding the address present at the first input to the relative address value present at the second input to form an address which is buffer-stored in the base address register.

The prior art of record teaches an address generator comprising a base address counter and a plurality of offset address generators where the base address counter is connected to an input of an addition circuit. The address generator furthermore contains a multiplexer circuit (second multiplexer), which, is dependent on a selection control signal and through-connects an offset address generator to a further input of the addition circuit. The addition circuit adds the address present at the first input to the relative address value present at the second input; Shim (US-6038692) is an example of such prior art. The prior arts of record, however, fail to teach, singly or in combination,

a first multiplexer circuit, which is dependent on a base register selection control signal and switches through an address buffer-stored in the base address register to a first input of an addition circuit and to an address bus, which is connected to the circuit to be tested. Also, the prior arts of record, however, fail to teach, singly or in combination, a second multiplexer circuit, which is dependent on the base register selection control signal and through-connects the offset register group associated with the through-connected base address register to a third multiplexer circuit. Furthermore, the prior arts of record, however, fail to teach, singly or in combination, a third multiplexer circuit that is dependent on an offset register selection control signal and through-connects an offset register of the through-connected offset register group to a second input of the addition circuit.

The Examiner agrees with the Applicant's arguments with regard to these features in view of the arts of record; therefore, the Examiner favors the allowance of claims 1-10. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
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